

09/483712

ABSTRACT OF THE DISCLOSURE

A chip-scale package and method for making same. A pattern of conductive traces in the form of lead fingers is adhered to the active surface of a semiconductor die, preferably using a dielectric tape. The conductive traces are wire bonded to bond pads of the semiconductor die to establish electrical connections therebetween. Discrete conductive elements are then attached to the conductive traces in a pattern corresponding to a terminal pad pattern on a carrier substrate such as a printed circuit board. The semiconductor die, tape, conductive traces, wire bonds and interior portions of the discrete conductive elements are encapsulated to create a completed chip-scale package having an array of conductive connections protruding through the encapsulant.

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